

FIG. 1

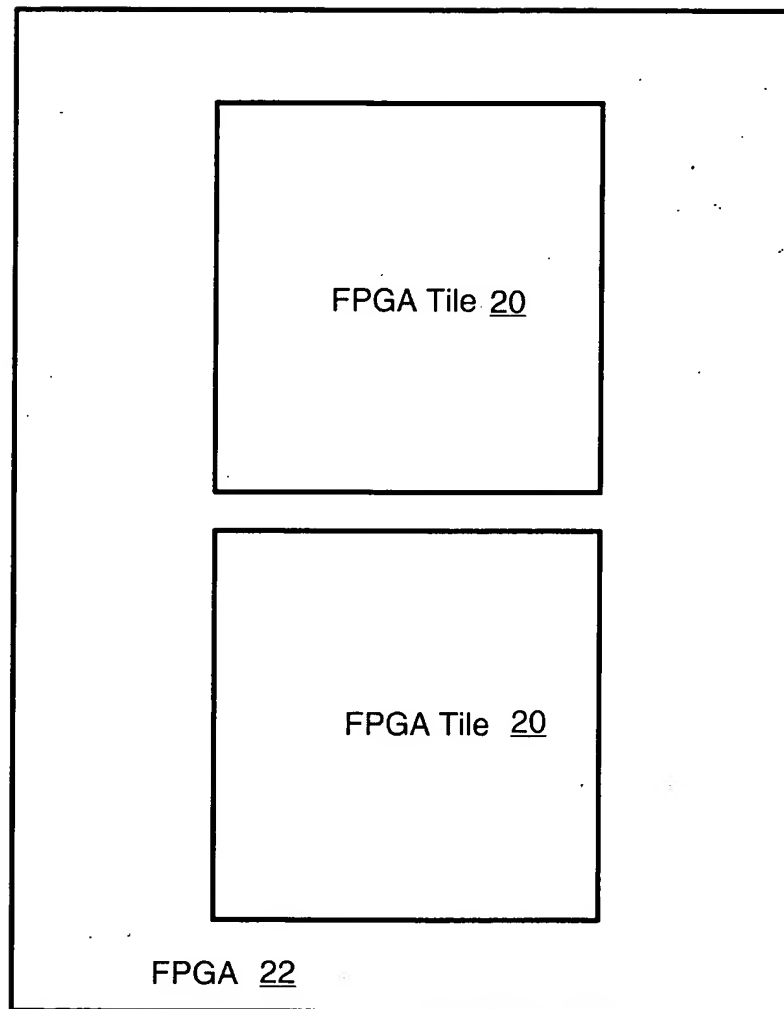


FIG. 2

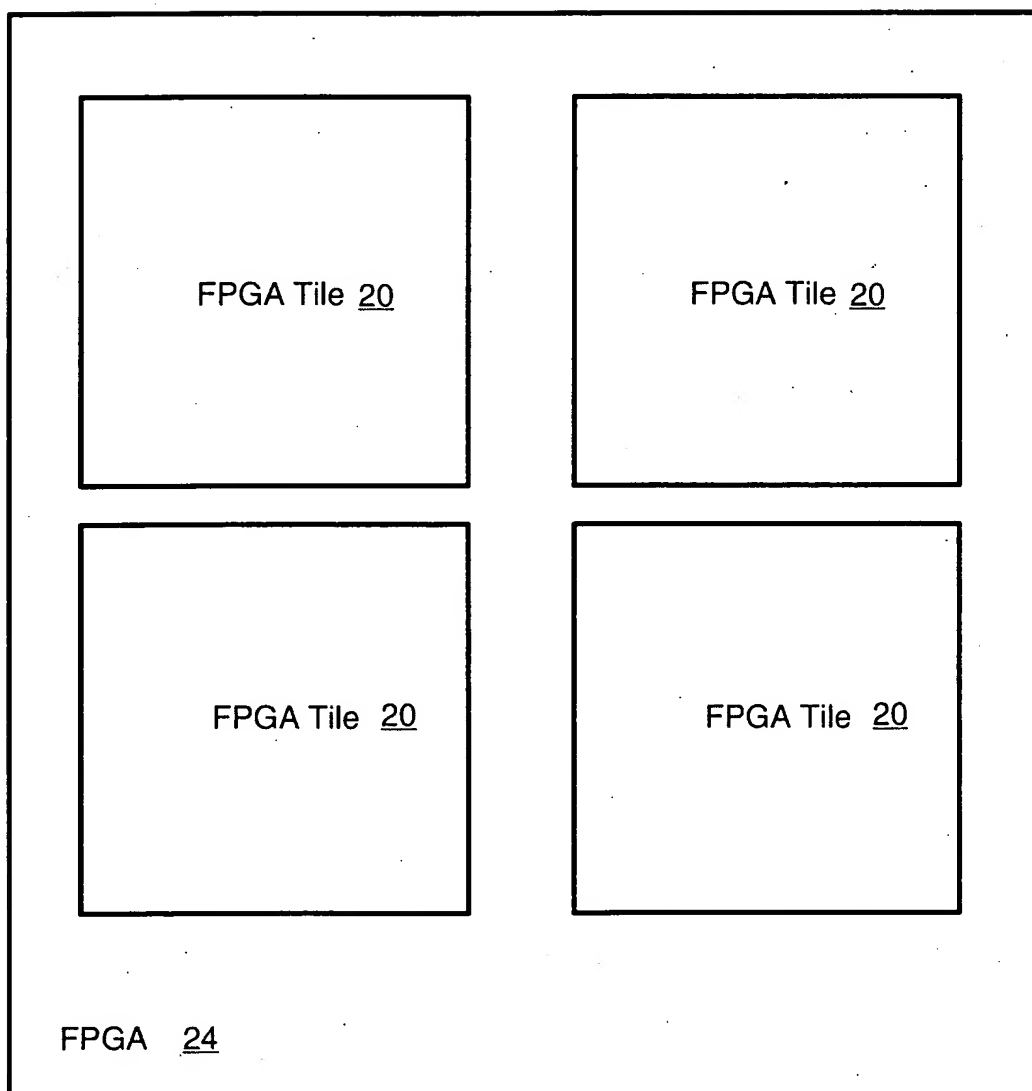


FIG. 3A

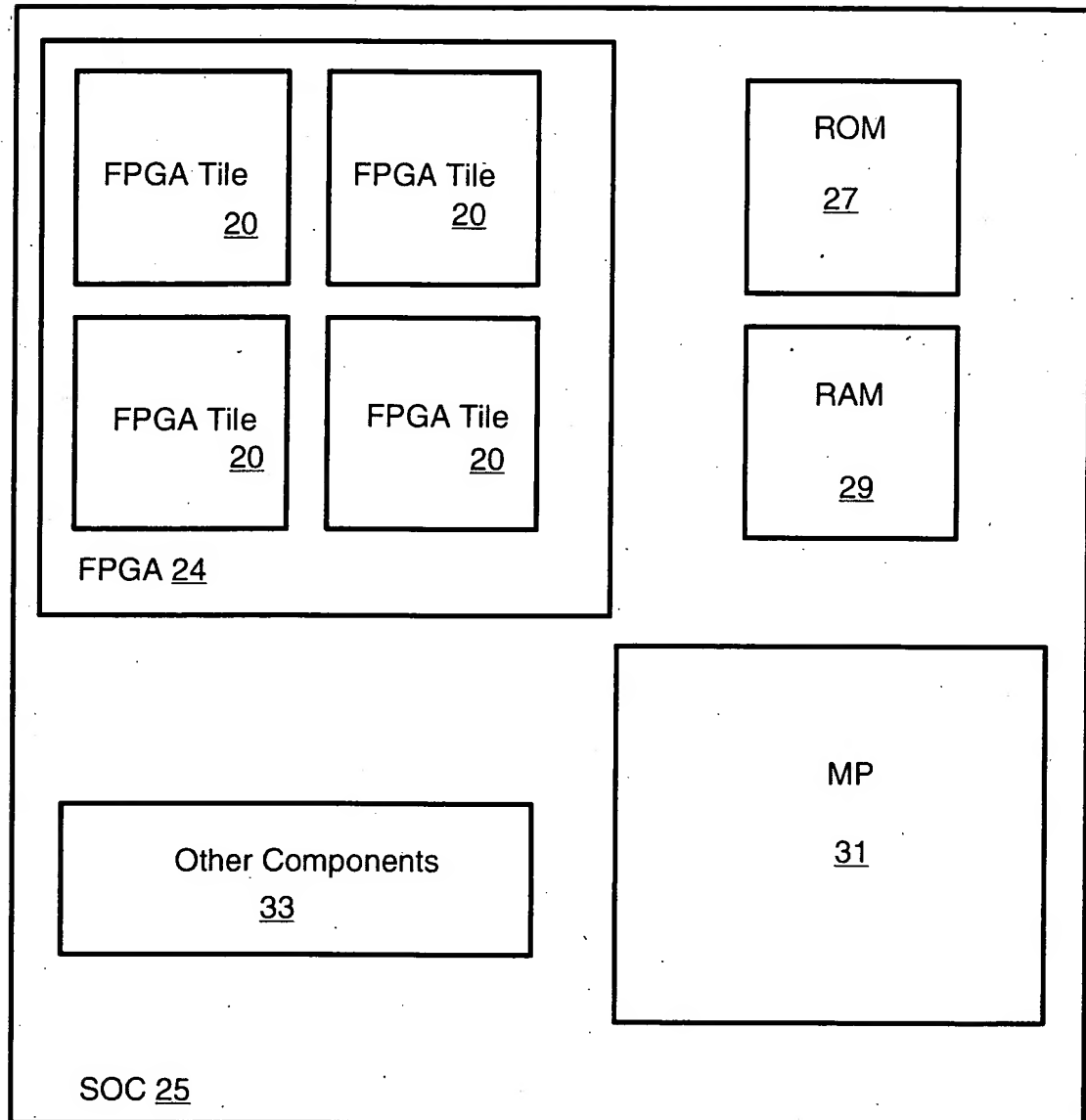


FIG. 3B

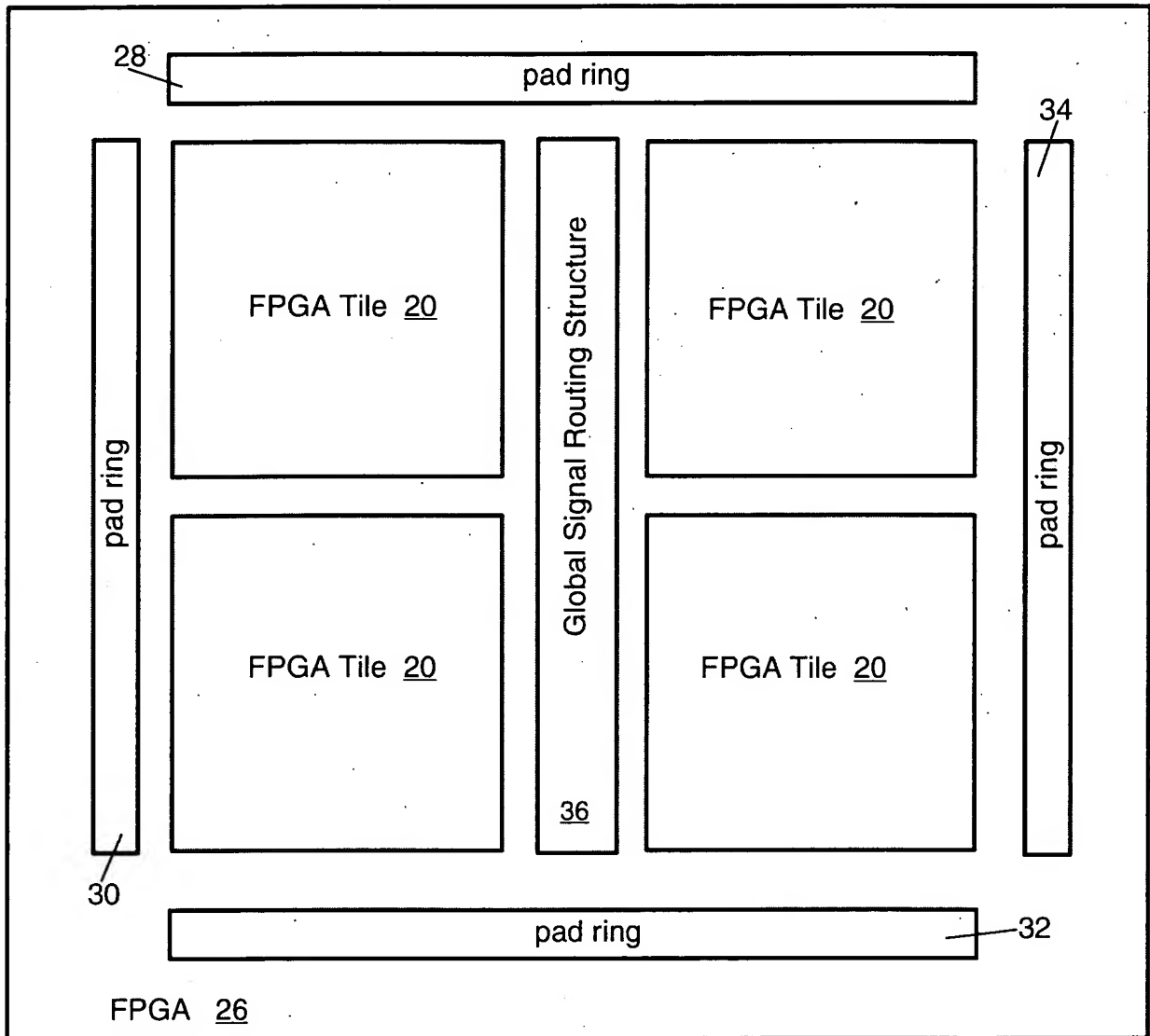


FIG. 4

20

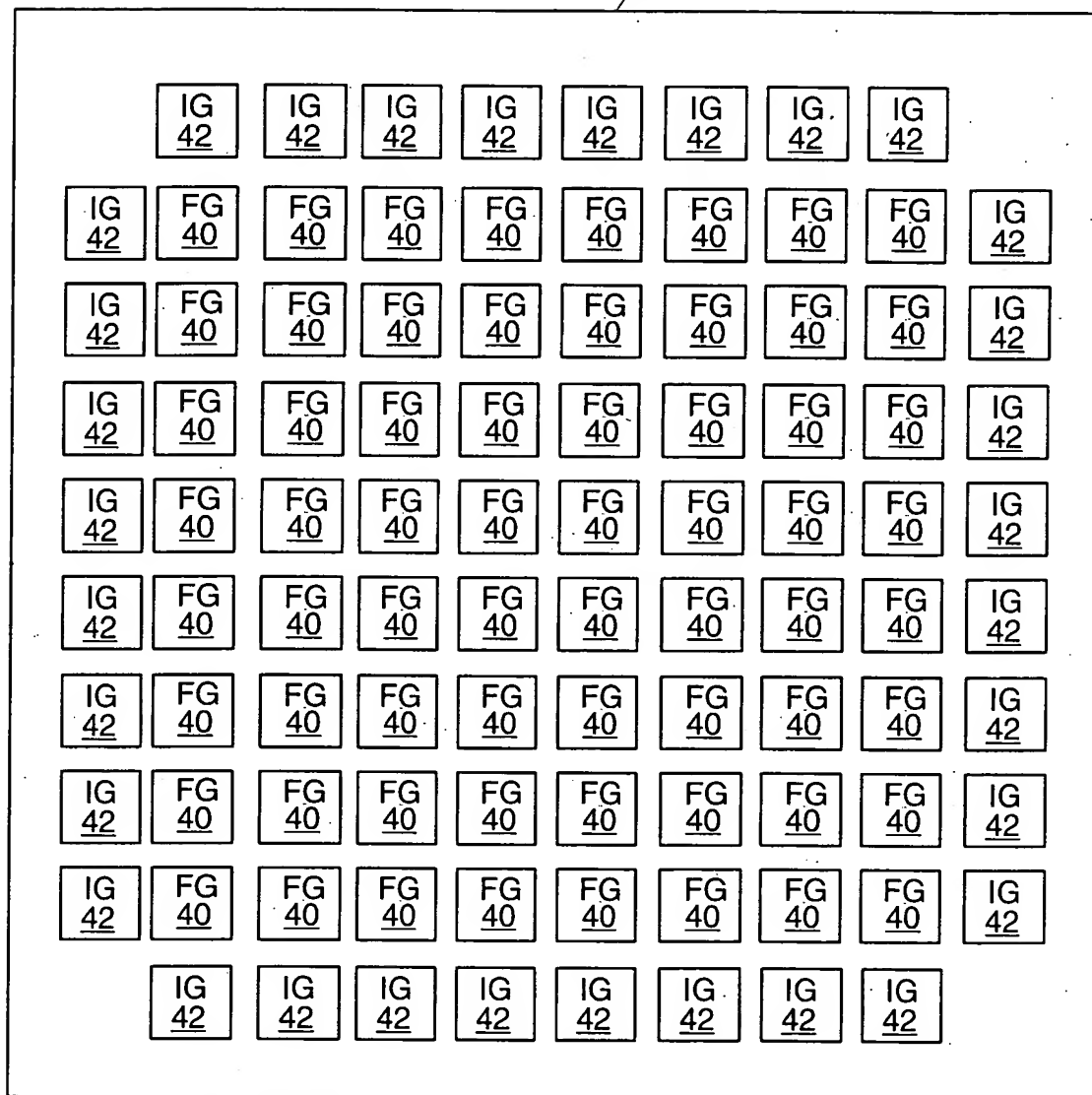


FIG. 5

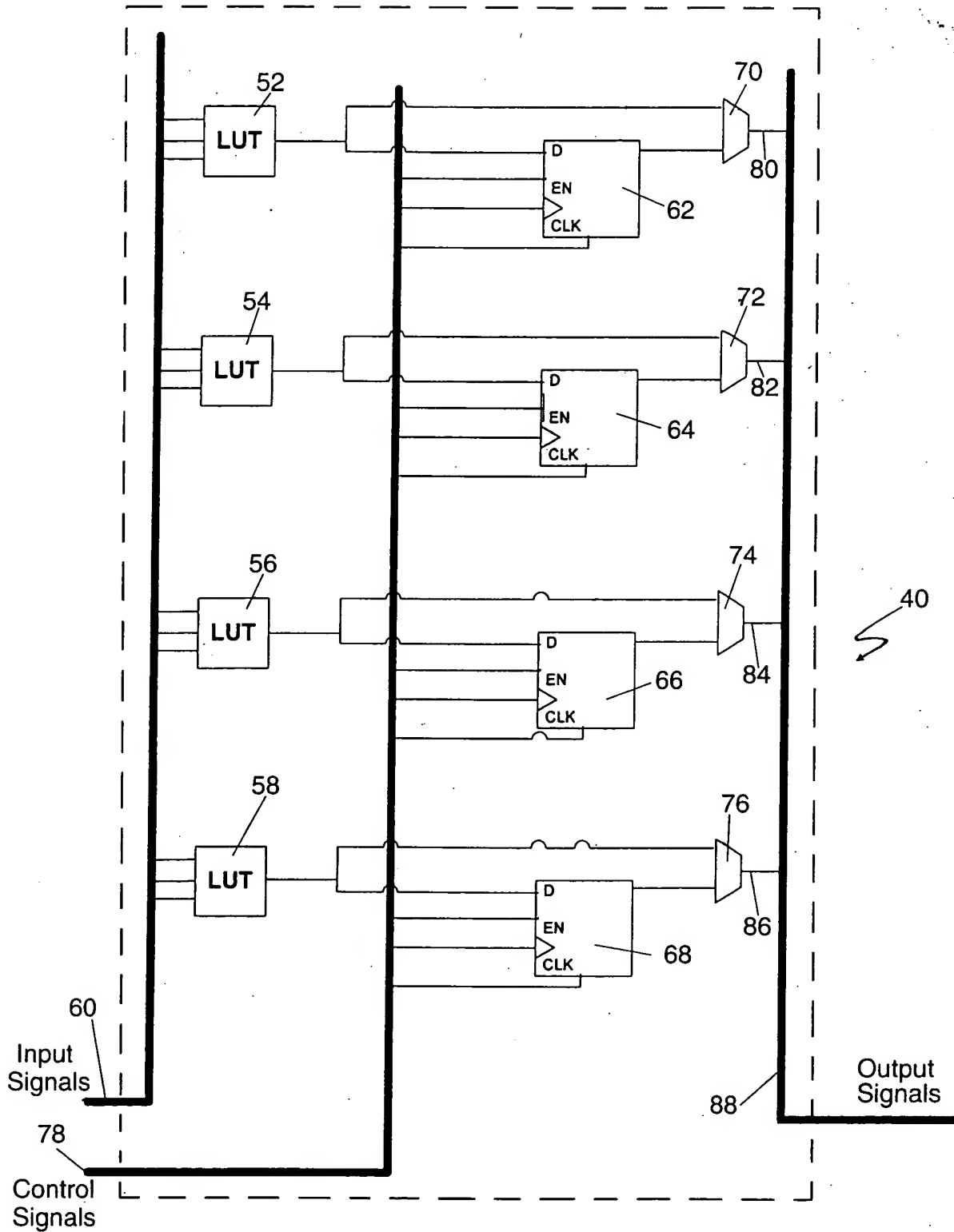


FIG. 6

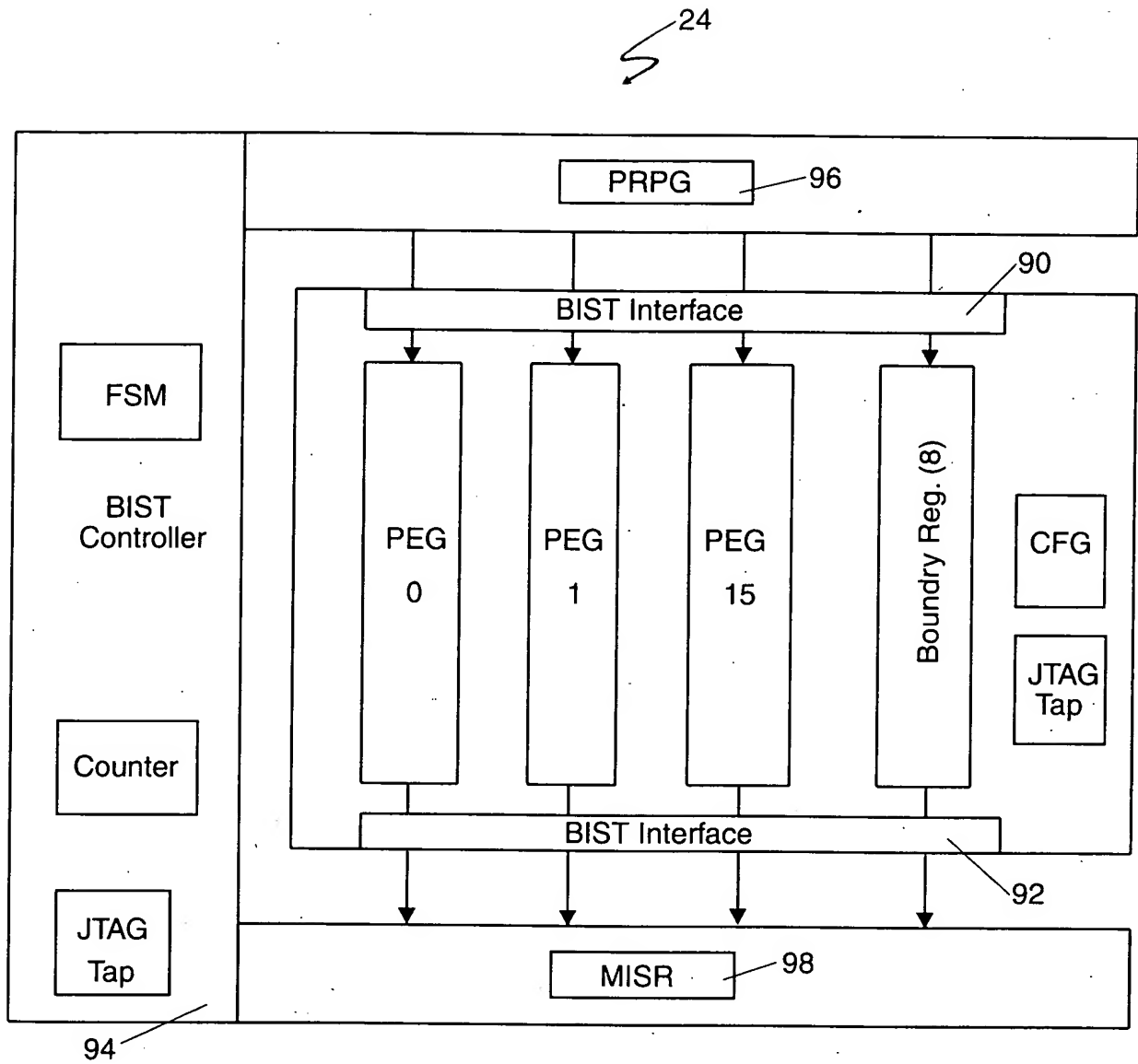


FIG. 7

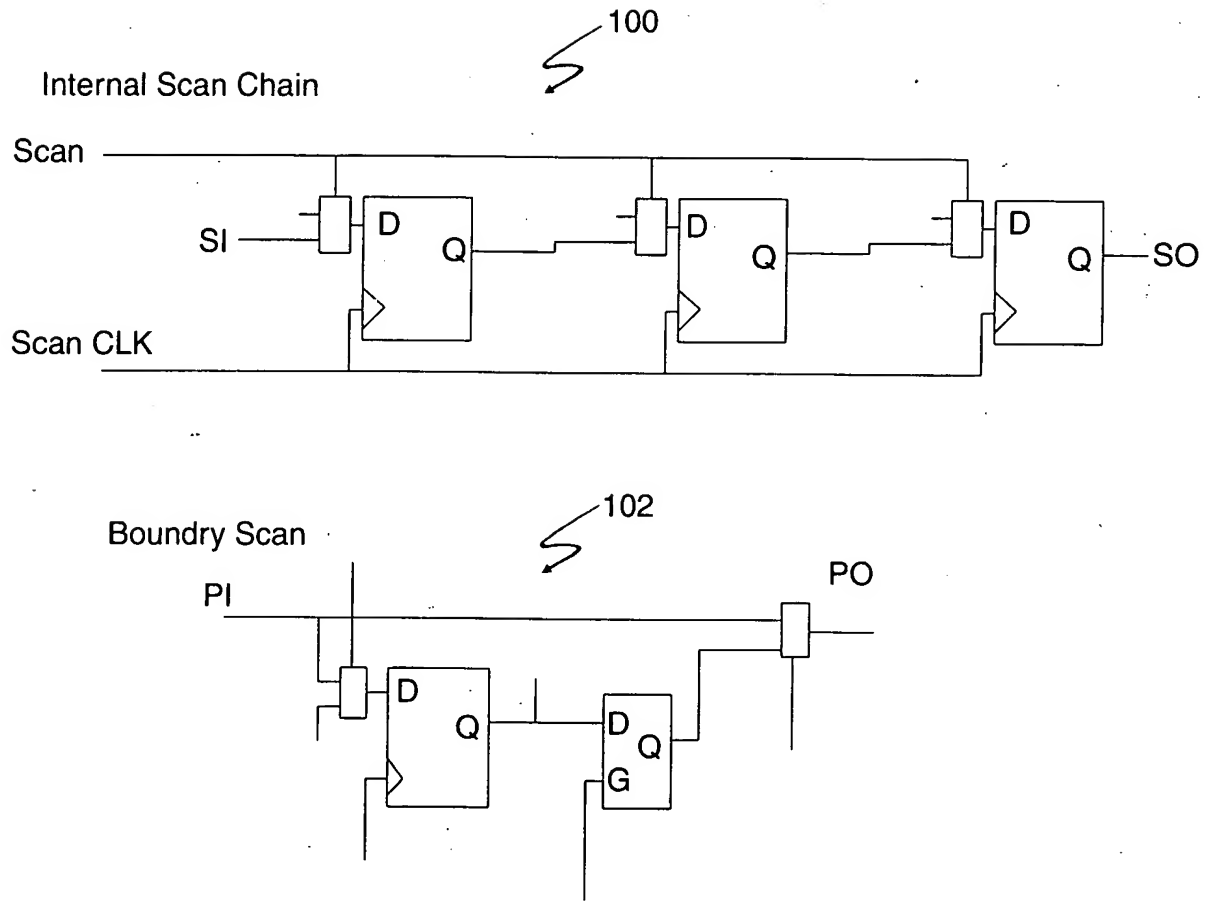
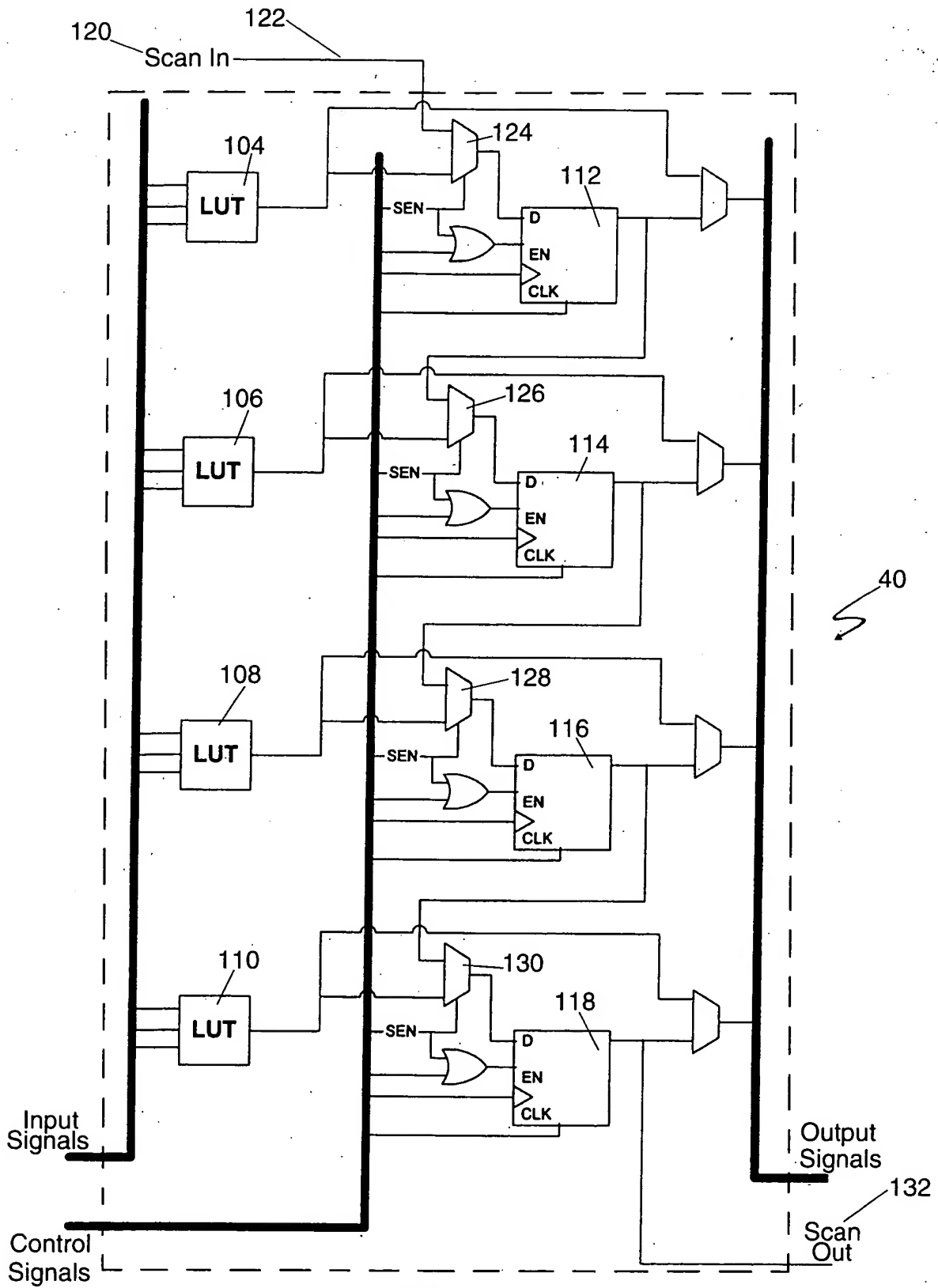


FIG. 8



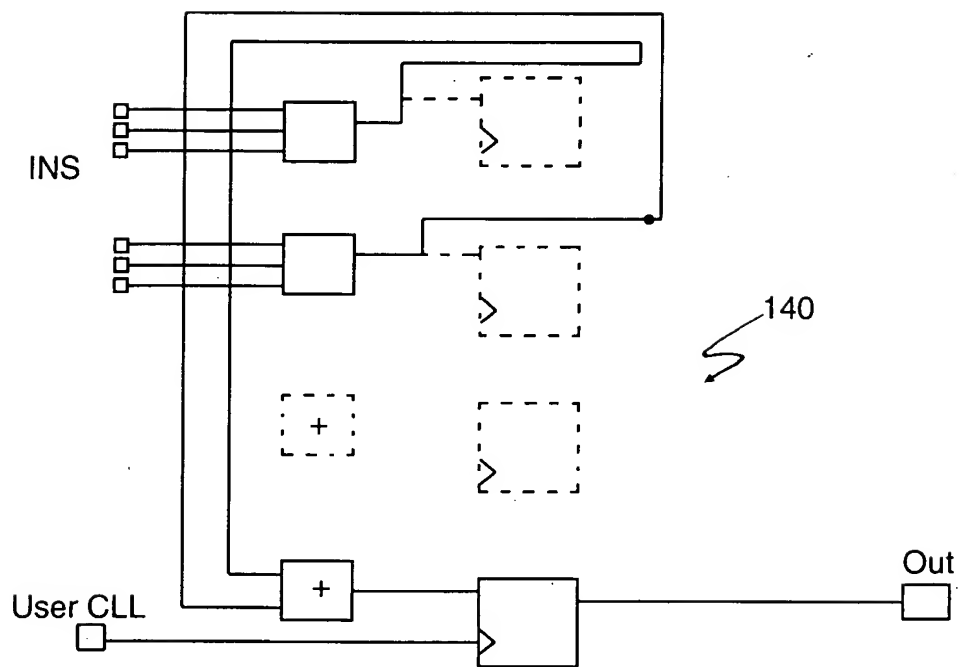


FIG. 10A

User Logic: Implementation of AND OR Circuit and Register

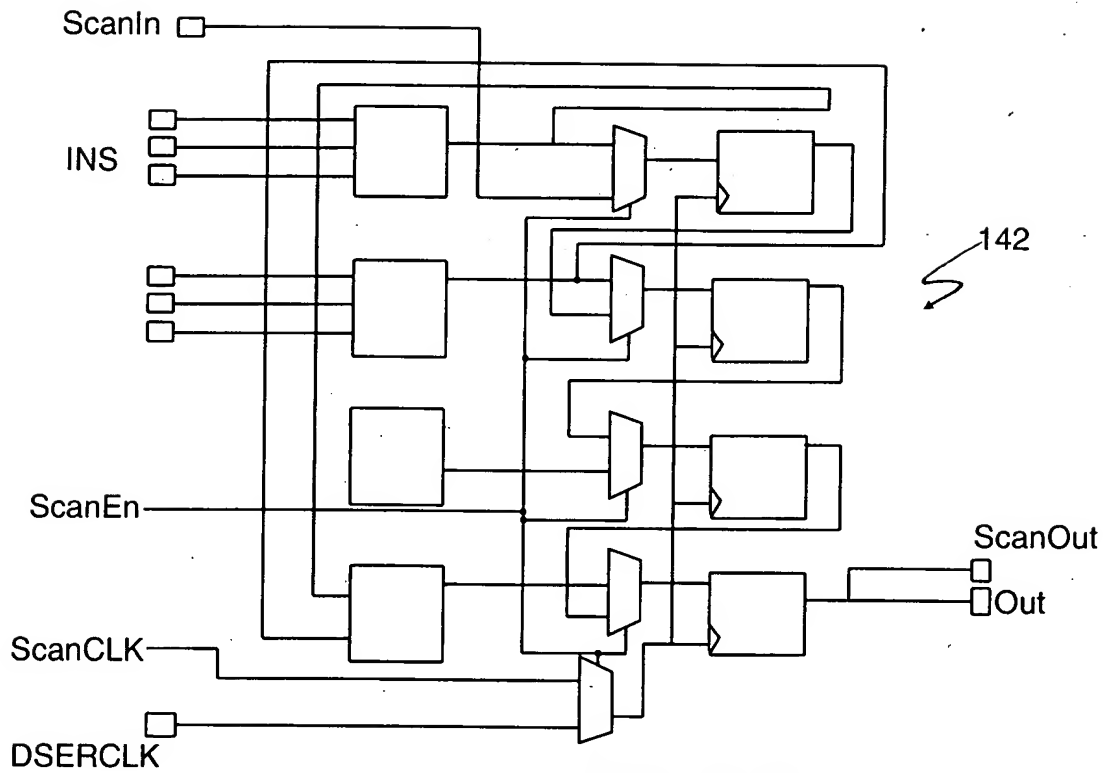


FIG. 10B

DSER Logic - with Scan Superimposed

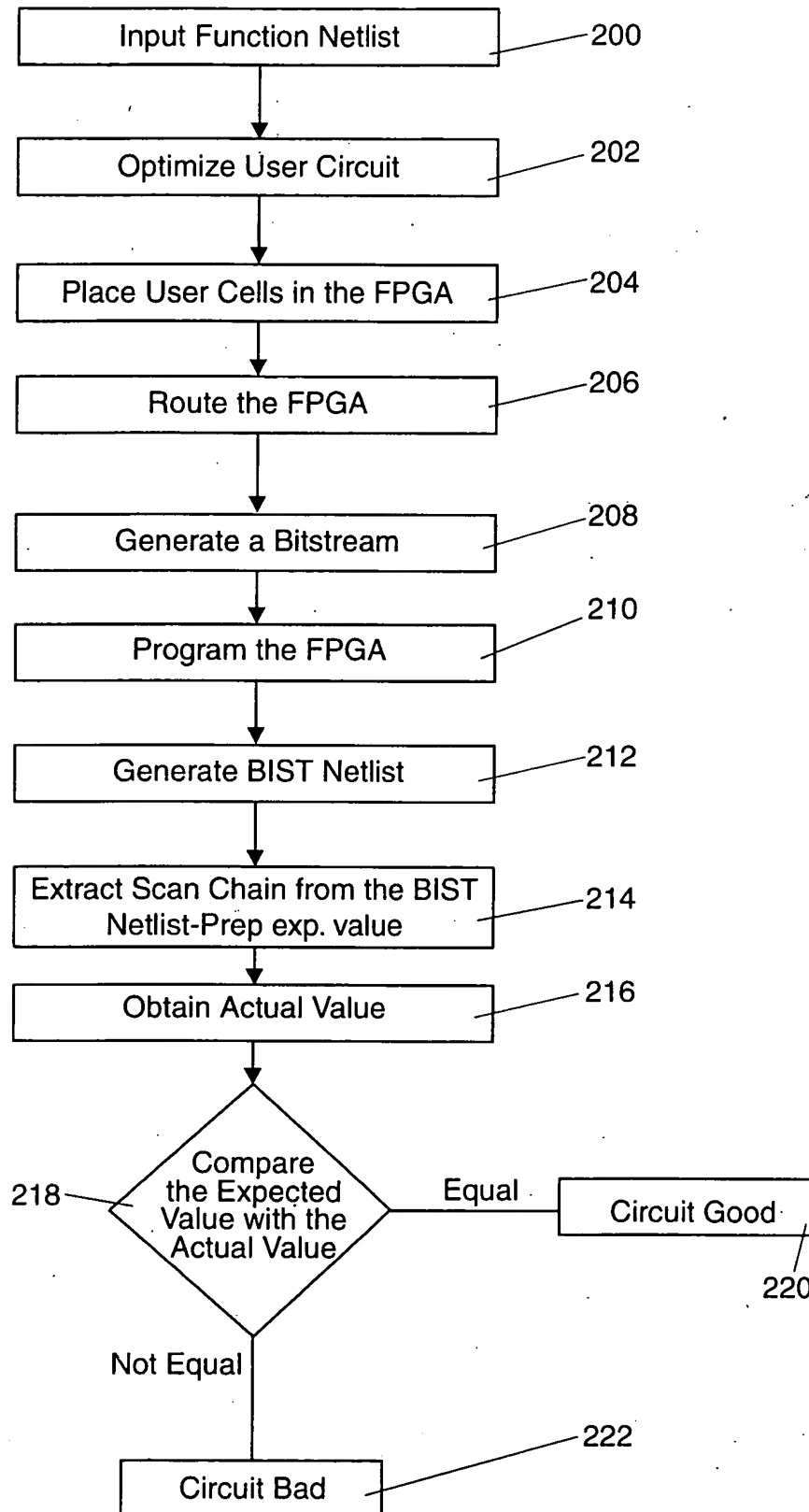


FIG. 11